CLAIMS:

1. A processing device for executing virtual machine instructions; the processing device comprising:

an instruction memory for storing instructions including at least one of the virtual machine instructions;

a microcontroller comprising a processor comprising a predetermined microcontroller core for executing native instructions from a predetermined set of microcontroller specific instructions; the native instructions being different from the virtual machine instructions; and

a pre-processor comprising:

a converter for converting at least one virtual machine instruction, fetched from the instruction memory into at least one native instruction; and

feeding means for feeding native instructions to the microcontroller core for execution;

characterised in that:

the processor is of a type which after the occurrence of a predetermined condition, such as an interrupt, requests re-feeding of up to a predetermined maximum of **n** native instructions, where $n > 1$; and

the feeding means comprises means for in response to the processor requesting re-feeding of a number of native instructions, re-feeding the requested native instructions.

2. A processing device as claimed in claim 1, characterised in that the pre-processor comprises a feeding memory for storing at least **n** instructions which were last fed to the processor; and

in that the feeding means is operative to, in response to the processor requesting re-feeding of a number of instructions, re-feeding the requested instructions from the feeding memory.

3. A processing device as claimed in claim 2, wherein the microcontroller is of a pipelined architecture, with a **k**-stage pipeline and **n** is equal to or larger than **k**.

4. A processing device as claimed in claim 2, wherein the processor

comprises an instruction cache for storing up to **h** instructions and **n** is equal to or larger than **h**.

5. A processing device as claimed in claim 2, wherein the microcontroller is of a pipelined architecture, with a **k**-stage pipeline, and the processor comprises an instruction cache for storing up to **h** instructions; and **n** is equal to or larger than **k + h**.

6. A processing device as claimed in claim 2, wherein the feeding memory comprises locations for storing at least **n + m** native instructions, where **m** $\geq$ 1 and the pre-processor is operative to generate and store in the feeding memory up to **m** native instructions for first-time feeding to the processor.

7. A processing device as claimed in claim 6, wherein instructions to be successively fed or re-fed to the processor are stored successively; and the pre-processor comprises:

a counter indicating an address of an instruction expected to be requested next by the processor for first time feeding;

means to determine an offset of an actual address of an instruction requested by the processor with respect to the address stored in the counter; and

based on the offset locating the requested instruction in the feeding memory.

8. A processing device as claimed in claim 1, characterised in that the pre-processor comprises storing means for storing a state of the pre-processor enabling to regenerate at least **n** instructions which were last fed to the processor; and

in that the feeding means is operative to, in response to the processor requesting re-feeding of a number of instructions, re-feeding the requested instructions by regenerating the instructions based on the stored state.

9 A processing device as claimed in claim 8, characterised in that the storing means is operative to store at least part of the state in an instruction pointer of the microcontroller; and in that the feeding means is operative to retrieve the stored part from the instruction pointer.

10. A processing device as claimed in claim 9, characterised in that the pre-processor comprises for at least one virtual machine instruction a corresponding translation table for translating the virtual machine instruction into a sequence of native instructions; the table comprising native instructions and/or native instruction skeletons; in that the state comprises a translation table offset indicator; and in that the storing means is operative to store the translation table offset indicator in a predetermined least-significant part of the

instruction pointer of the microcontroller; and in that the feeding means is operative to locate a native instruction or a native instruction skeleton in the translation table under control of the translation table offset indicator in the instruction pointer.

11. A processing device as claimed in claim 10, characterised in that the state further comprises a virtual machine instruction pointer indicating a virtual machine instruction in the instruction memory; and in that the storing means is operative to store the virtual machine instruction pointer in a predetermined further part of the instruction pointer of the microcontroller; and in that the pre-processor comprises means for fetching a virtual machine instruction from a location in the instruction memory indicated by the virtual machine instruction pointer in the instruction pointer of the microcontroller, and in that the feeding means is operative to locate the translation table corresponding to the fetched virtual machine instruction.

12. A processing device as claimed in claim 10, characterised:

in that the translation table is divided into a plurality of sub-tables, at least one of the sub-tables comprising a sequence of native instructions or native instruction skeletons;

in that the translation table offset indicator indicates an offset in a sub-table;

in that the state further comprises a sub-table indicator; and in that the storing means is operative to store the sub-table indicator in a predetermined further part of the instruction pointer of the microcontroller;

and in that the feeding means is operative to locate a native instruction or native instruction skeleton at a location in the sub-table indicated by the sub-table indicator of the instruction pointer and the translation table offset indicator of the instruction pointer.

13. A processing device as claimed in claim 1, wherein the microcontroller comprises the instruction memory and the pre-processor; the processor, instruction memory and pre-processor being coupled via an atomic-transaction microcontroller bus; the microcontroller being of a type requesting (re-)feeding of a native instruction via the bus and the pre-processor being operative to fetch a virtual machine instruction from the instruction memory via the bus for conversion to associated native instruction(s); and wherein the pre-processor comprises means for, in response to the processor requesting (re-)feeding of a native instruction whose associated virtual machine instruction is not or no longer present in the pre-processor, feeding a no-operation (NOP) instruction to the processor completing the bus transaction initiated by the processor.

14. A pre-processor for use with a microcontroller comprising a processor comprising a predetermined microcontroller core for executing native instructions from a predetermined set of microcontroller specific instructions;

the pre-processor comprising:

a converter for converting at least one virtual machine instruction, fetched from an instruction memory, into at least one native instruction; the native instructions being different from the virtual machine instructions; and

feeding means for feeding native instructions to the microcontroller core for execution;

characterised in that the feeding means comprises means for in response to the processor requesting re-feeding of more than one native instruction, re-feeding the requested native instructions.